ABSTRACT

A data processing device capable of high speed operation and shorter instruction processing time without causing software compatibility problems. When storing an instruction from the memory into the instruction cache memory and the instruction possesses a spare field, the instruction code of that instruction is predecoded in the predecode-processor and the information generated is stored in the spare field corresponding area of the instruction cache memory. When that instruction is fetched from the instruction cache memory, the information stored in the spare field corresponding area of the instruction cache memory is utilized. In this way, processing can proceed based on the predecoded information without having to await the completion of decoding of the instruction fetched from the instruction cache memory.